ABSTRACT OF THE DISCLOSURE

There are provided a base member 14, a position restriction mechanism 15, a height restriction mechanism 17, an evenness holding mechanism , and an alignment mechanism 20, 22. A plurality of semiconductor modules is serially layered on the base member. Each semiconductor module comprises a semiconductor chip 7 mounted on a printed-wiring board 6 and a bump 13 formed on an interlayer connection land 8. The position restriction mechanism 15 restricts respective positions of the semiconductor modules 2 to be layered on the base member 14. The height restriction mechanism 17 restricts the height of the entire layered semiconductor module unit 4 layered on the base member 14. The evenness holding mechanism maintains evenness of the semiconductor module 2. The alignment mechanism 20, 22 aligns a mother substrate 5 on which a multilayer semiconductor module unit 4 is mounted.